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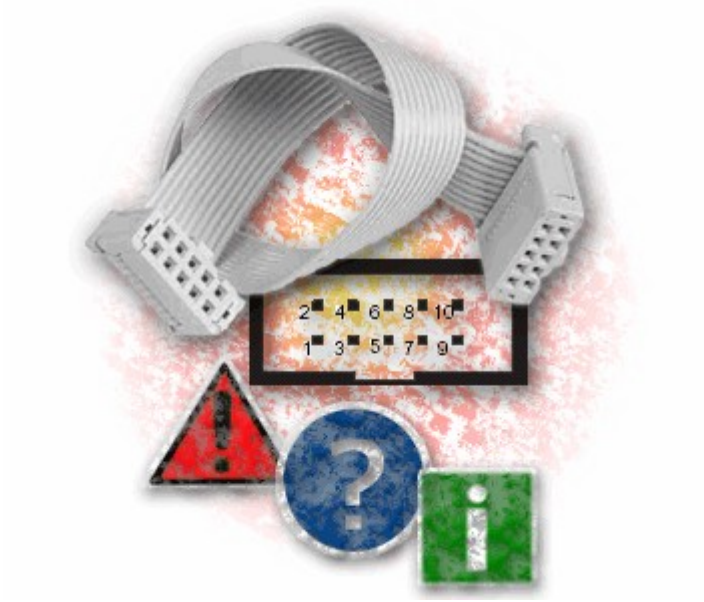
AN–ELNEC–EN–ISP–SEEP–SPI

# Application note for In-System Programming of SPI™ Serial memories



## General overview of serial memories

There exist a lot of variations of serial programmable memories, which can be divided by capacity *(from few bytes to mega bytes),* manufacturing technology *(EPROM, EEPROM, FLASH)*, organization *(x8, x16),* package type *(DIP, SOIC, TSSOP, MLF, SON, ...),* pins count and alignment, special features *(protection against inadvertent writes),* ... so **you should be familiar** with the device to know its operation and features before you start working with it.

Considering the ISP programming, the major aspect to sort serial memories, is a type of used communication protocol:

- *IIC™ (Inter Integrated Circuit),*
- *SPI™ (Serial Peripheral Protocol),*
- *MW™ (Micro Wire)*,
- *JTAG (Joint Test Action Group).*

This Application Note discusses the SPI serial EEPROM and FLASH memories.

# About SPI™ Serial memories

SPI is a type of bi-directional 3-wire communication protocol. There must be only one device acting as slave, and one acting as master, active on the same bus at the same time.

Activation/deactivation of current slave SPI memory is done by setting its ***CS*** *(Chip Select)* signal to appropriate level. This signal can not be static during ISP operation, so it needs to be driven from ISP programmer.

The communication interface represent signals *SI (Serial Data Input), SO (Serial Data Output) and SCK (Serial Clock).*

Most of SPI devices have HW write protection capability applicable on device memory. While the *WP\ (Write Protect)* signal is active, all write operations are inhibited, and the data inside can not be altered.

SPI EEPROM memories have ***HOLD*** pin, which allows master to pause serial sequence without resetting it. SPI Serial Data Flash memories have **RESET** input, which can terminate currently running process and reset internal state machine, and **SER/PAR** input, which allows user to choose serial or parallel communication mode.

*VCC* and *GND* are used to supply voltage connection.

For further informations about all memory features, please refer to technical specification of your SPI serial memory – *Datasheet (DS).*

## Signals:

| *Pin name* | *Function* | *Description* | *Signal level* |
|---|---|---|---|
| VCC | power | device power supply | 1.8–5.5 (V) |
| GND | | common ground | 0 (V) |
| WP\ | control | Write Protect input | H, L |
| CS\ | | Chip Select input | |
| HOLD\ | | Hold input | |
| RESET\ | | Reset input | |
| SER/PAR\ (SER/BYTE\) | | Communication mode select input | |
| SI, SO | communication | data input, output respectively, standard CMOS | L, H, Pull-Up |
| SCK | | clock signal, standard CMOS | H, L |
| NC | – | not connected | – |
| DC | – | don't connect | – |

*Table 1. SPI device signals description*

## Pinouts:

### *SPI Serial EEPROM memories*

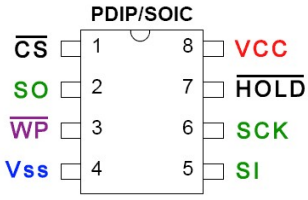



*Figure 1. Standard pinout*

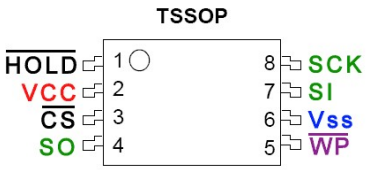



*Figure 2. Rotated pinout*

### *SPI Serial Data Flash memories*

Please, take a look at datasheet of your serial memory, to make sure, the pinout is correct and device is connected properly. The Figures 3-8 are applicable only to Atmel AT45 series.

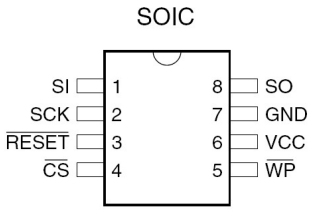



*Figure 3. Standard SOIC8 pinout*

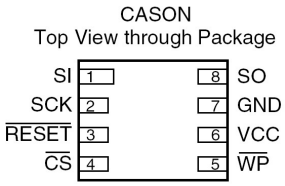



*Figure 4. Standard CASON8 pinout*

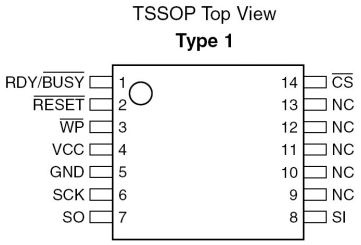



*Figure 5. Standard TSSOP14 pinout*

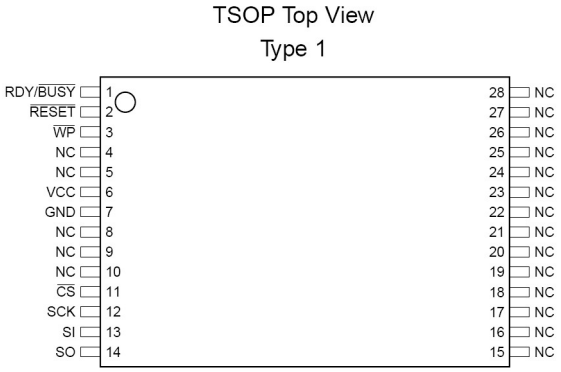



*Figure 6. Standard TSOP28 pinout*

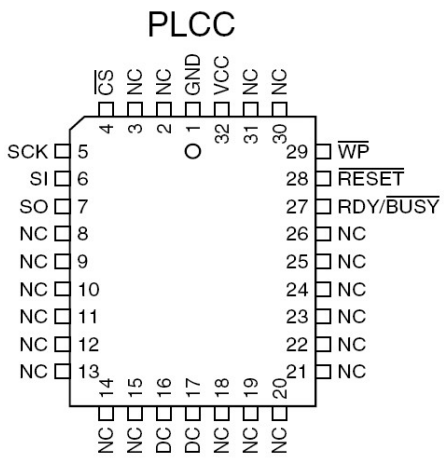



*Figure 7. Standard PLCC32 pinout*

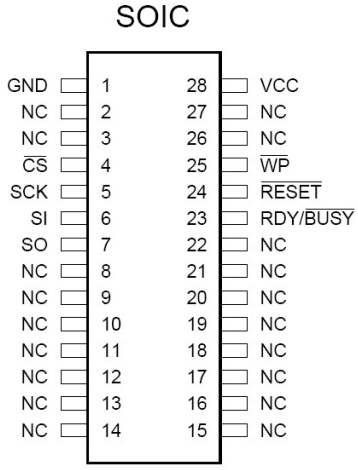



*Figure 8. Standard SOIC28 pinout*

## Adaptation of target system for ISP

Following text contains **important notices** related to correct ISP connection of in-system programmed EEPROM/FLASH memory.

Respecting this, may prevent you from undesirable signal interference on pins *SI, SO, SCK* of programmer and target system which often results in unsuccessful course of ISP operation.

Detailed information about ISP pin-driver capability and pins assign is listed in control program **PG4UW** of programmers *(see Figure 12).*

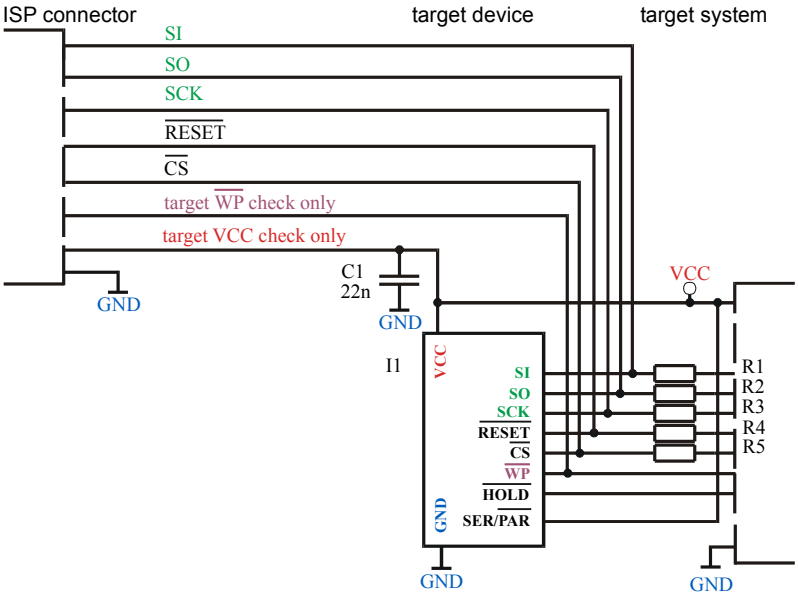



*Figure 9. Circuit design*

**SI, SO, SCK, CS\, *RESET\–** These pins are internally connected as standard CMOS input or output. It means, that none of these signals must be pulled up, as it is in case of *IIC* serial memories. Resistors R1, R2, R3, R4, R5 with value 10kΩ should be used to isolate signals of programmer and target system. Otherwise the device may have problems with signal level recognition.

**WP\ –** Write Protect pin, must be set to inactive level while programming the device. The programmer uses this signal to test the WP\ pin level before programming the chip.

***HOLD\ –** Hold pin, if is implemented, **must be set to inactive level** while operating with device. Otherwise, the memory will ignore programmers commands and some operations will run incorrectly, although it could seem to be successful *(e. g.: Blank check)*. The programmer does not check level of this signal.

***SER/PAR\ (SER/BYTE\) –** Serial/parallel mode select input pin, if is implemented, **must be set to H level (serial mode)** while operating with device. The programmer does not check level of this signal.

* - pins might not be implemented

**VCC –** Power supply for programmed device must be supplied from target system. The programmer uses this signal only to test, if the target memory is powered. You can omit to connect this signal, and disable VCC sense.

**GND –** Common ground for programmer and target system.

# Operating with device

## Device operation options:

Most of the programmers offer an option to supply power for target system. If you want to use it, you must set up at least basic parameters. You can do it through menu *Device Options <Alt+O> - in next <Alt+O> (see Figure 10).*

Voltage level limitation of logical *H* signal is derived from target memory *VCC*, set in *Supply voltage* edit box *(value 3300mV, Figure 10)*.

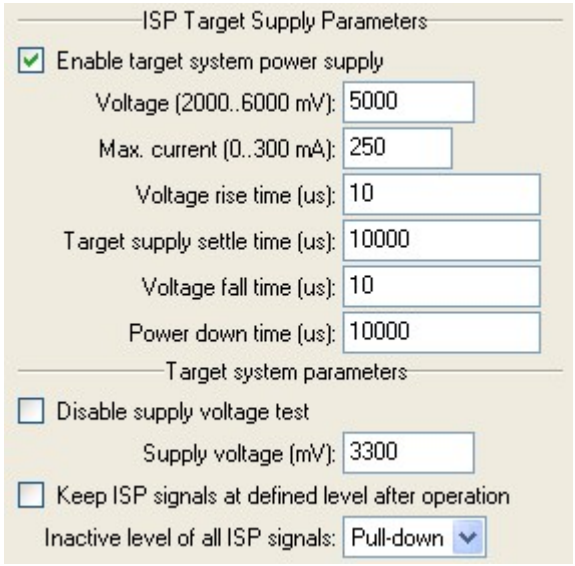



*Figure 10. ISP target supply parameters setting <Alt+O>*

In case of unfavourable communication conditions (longer wires, interfering environment, interference between signal from programmer and system...) you can decrease clock frequency used for communication by predefined steps *(see Figure 11)*. Default value is set to maximum supported by selected memory.

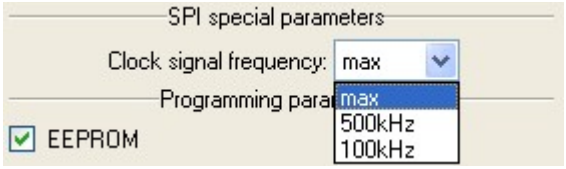



*Figure 11. SPI special parameters setting <Alt+O>*

For further description of ISP parameters, please take a look at menu *Help* by pressing the <*F1*> key, while the window <*Alt+O*> is opened.

## Device info (Ctrl+F1):

The following window contains reduced information from this application note and details about pins assign for each programmer with short description of circuit design *(see Figure 9).*

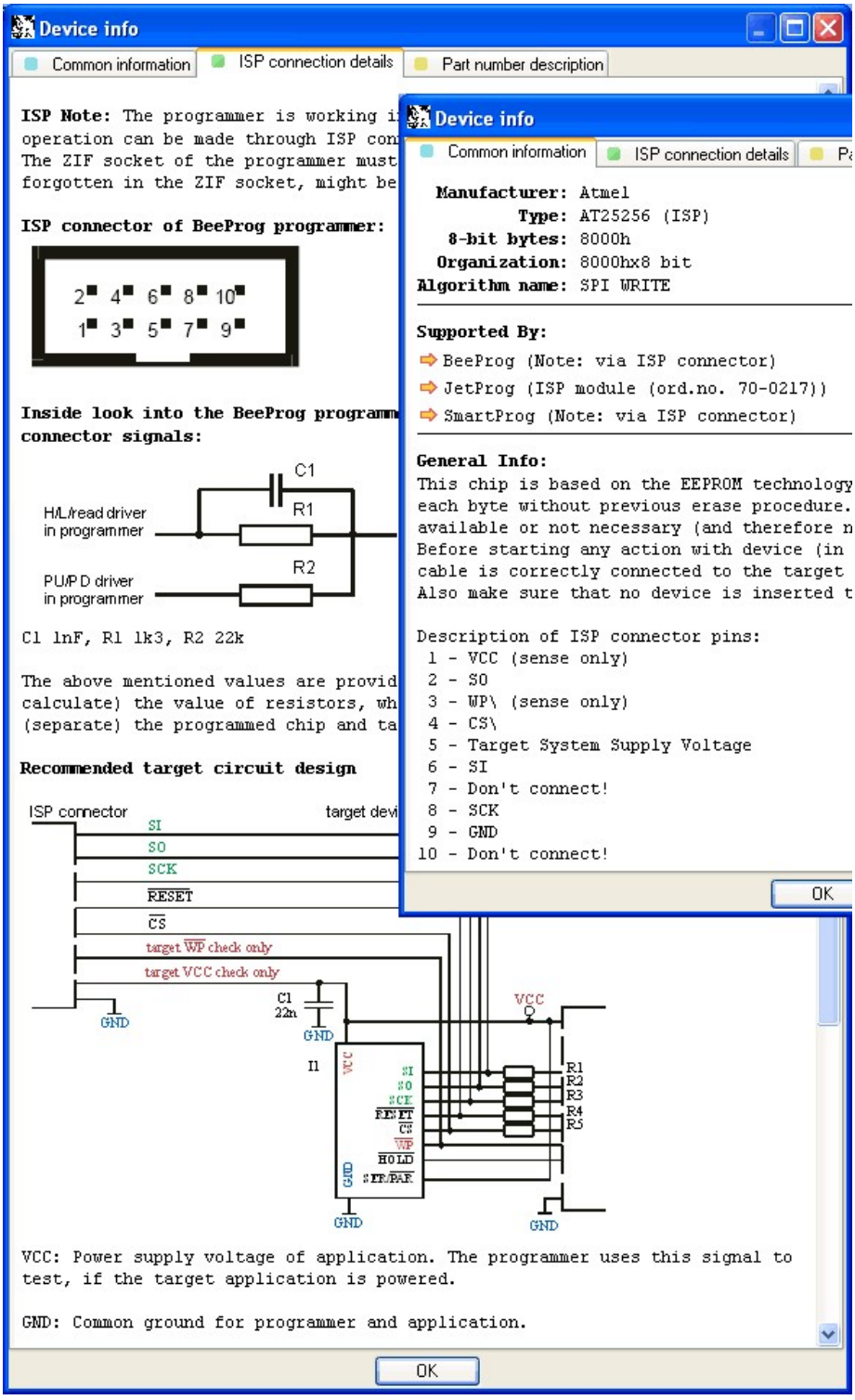



*Figure 12. Device info*

## Connecting programmer to system:

**Turn off power supply of system** before connecting/ disconnecting programmer to/from system.

## Before starting an operation:

Before starting an operation with target memory, please make sure, that the **ISP cable is correctly connected** to the target system and programmer. Also make sure that no device is inserted to *ZIF* socket of the programmer.

The ***HOLD*** signal must be inactive during each operation.
If you want to program the device, please make sure, that **signal *WP* will not be active** during the action.

**Details about pins assign for each programmer** and short description of circuit design can be found in control program (*Device Info <Ctrl+F1>).*

Device pins marked *NC (Not Connected)* or *DC (Don't Connect!)* should be left unconnected. Also leave unconnected the pins of ISP connector marked ***"Don't Connect!".***

Correctly isolated signals of SPI bus can provide reliable signal level recognition (for both, programmer and system) and successfulness of desired operation. Please make sure, that your design meets our recommendations (see also *Adaptation of system for ISP,* page 4).

## If something went wrong:

If programmer reports **signal interference error,** may be, a signal interference occurred between programmer and system. Please make sure, your design meets our recommendations. Check the value of isolating resistors on *SI, SO, SCK, CS*\ wires.

If operation result still reports errors, please try to **decrease clock frequency** and repeat last operation *(<Alt+O>).*

Be aware, that longer ISP cable (longer than 20cm/0,7ft) may cause an unpredictable signal interference. Make sure you are using correct cable.

## Used abbreviations

**AN –** *Application Note*.
**DIP, SOIC, TSSOP, MLF, SON –** type of device package.
**EEPROM –** *(Electrical Erasable Programmable Read Only Memory)* type of memory.
**HW WP –** *(Hardware Write Protect)* write protect feature. It's realized via appropriate signal level on device pin, not by setting some WP register.
**IIC™ –** *(Inter Integrated Circuit)* type of communication protocol, communication bus, IIC–bus™ is registrated trademark of *Philips Semiconductors Corporation.*
**ISP –** *(In System Programming)* programming of device inserted into system.
**JTAG –** *(Joint Test Action Group)* an acronym for Joint Test Action Group, is the usual name used for the IEEE 1149.1 standard for Test Access Port and Boundary Scan, primarily used for testing integrated circuits, but also useful as a mechanism for debugging embedded systems.
**MW™ –** *(MicroWire)* type of communication protocol, MICROWIRE™ is registrated trademark of *National Semiconductor, Corp.*
**Open collector/drain –** type of used interface, collector/drain of transistor creates an output. In order to be output able to set H level, the device needs to be supplied with constant PU on the pin.
**Pull–Up (PU)/Pull–Down (PD) –** *increase/decrease of signal level by connecting PU/PD* resistor to *VCC/GND*.
**SPI™ –** *(Serial Peripheral Interface)* type of communication protocol, SPI™ is registrated trademark of *Motorola Corporation.*
**ZIF –** *(Zero Insertion Force)* type of socket, used in programmer for better manipulation with device.

## Revision history

### 05/2006:

Changes of figures:

- *Fig. 9 Circuit design – minor changes*
- *Fig. 12 Device info– minor changes*

### 07/2005:

- added SER/PAR\ pin, thus updated *Table 1*, *Figure 9* and description.

### 06/2005:

Initial Release.