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AN–ELNEC–EN–ISP–SEEP–IIC

Application note for In-System Programming of IIC™ Serial EEPROMs

General overview of serial memories

There exist a lot of variations of serial programmable memories, which can be divided by capacity *(from few bytes to mega bytes),* manufacturing technology *(EPROM, EEPROM, FLASH)*, organization *(x8, x16),* package type *(DIP, SOIC, TSSOP, MLF, SON, ...),* pins count and alignment, special features *(protection against inadvertent writes),* ... so **you should be familiar** with the device to know its operation and features before you start working with it.

Considering the ISP programming, the major aspect to sort serial memories, is a type of used communication protocol:

- *IIC™ (Inter Integrated Circuit),*
- *SPI™ (Serial Peripheral Protocol),*
- *MW™ (Micro Wire)*,
- *JTAG (Joint Test Action Group).*

This Application Note discusses the IIC serial EEPROM memories.

About IIC™ Serial EEPROMs

IIC is a type of bi-directional 2-wire bus for inter-IC control. Each device connected to the bus is recognized by a unique address *[A2, A1, A0]* which is transmitted as a part of control word and compared with signal levels on hard wired pins *(A2, A1, A0) of device*.

The communication interface of IIC devices represents signals *SDA (Serial Data) and SCL (Serial Clock)*, which are internally connected as open collector (open drain). It means, that *SDA* and *SCL* wires of IIC bus needs to be driven with *pull-up* resistor *(PU),* to get ability to provide *H* level.

Some IIC devices have HW write protection capability applicable on device memory. While the *WP (PRE, WC\)* signal is active, the data inside of protected area can not be altered. For further informations about write protected address range, please refer to technical specification of programmed EEPROM – *Datasheet (DS).*

VCC and *GND* are used to supply voltage connection.

Signals:

Pin name	*Function*	*Description*	*Signal level*
VCC	power	device power supply	1.8–5.5 (V)
GND		common ground	0 (V)
WP (PRE, WC\)	control	Write Protect (PRotect Enable, Write Control)	H, L
A2, A1, A0		device system address	H, L
SDA	communication	data input/output, open collector (open drain)	L, Pull-Up
SCL		clock signal, open collector (open drain)	
NC	–	not connected	–
DC	–	don't connect	–

Table 1. IIC device signals description

Pinouts:

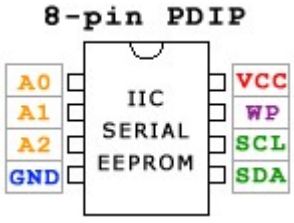

Figure 1. Standard pinout

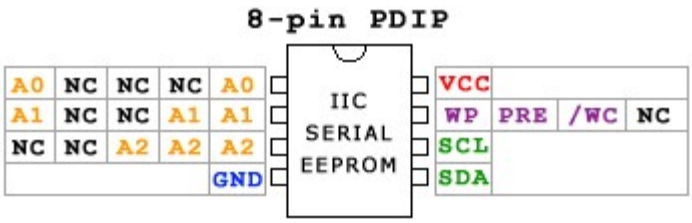

Figure 2. Alternative pinouts

Adaptation of target system for ISP

Following text contains **important notices** related to correct ISP connection of in-system programmed EEPROM.

Respecting this, may prevent you from undesirable signal interference on pins *SDA/SCL* of programmer and target system which often results in unsuccessful course of ISP operation.

Detailed information about ISP pin-driver capability and pins assign is listed in control program **PG4UW** of programmers (*see Figure 6*).

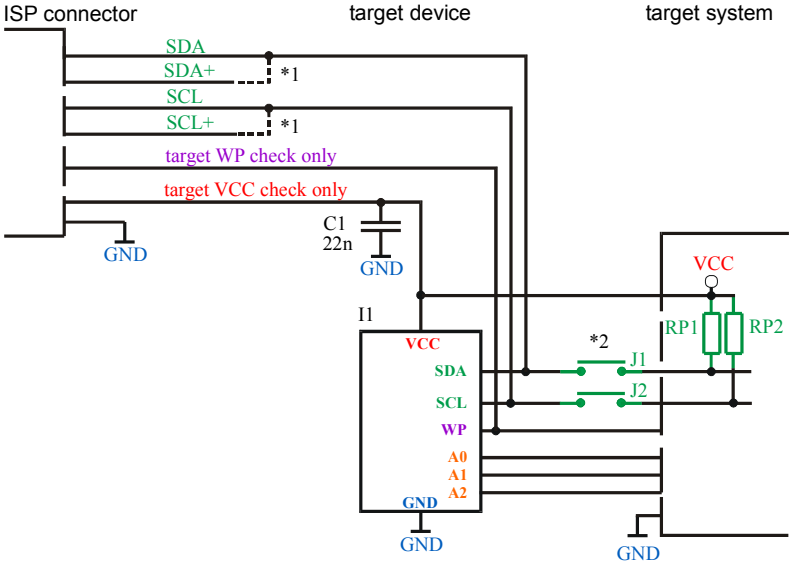

Figure 3. Circuit design

SDA, SDA+, SCL, SCL+ – These pins have to be driven with *pull-up* resistors RP1, RP2. Values must meet the IIC bus specification, otherwise the device may have problems with signal level recognition.

(*1): The programmer can provide a "stronger" ("better L level") *SDA/SCL* signals from ISP driver, by interconnecting of coupled signals *SDA, SDA+* and *SCL, SCL+.*

(*2): If you have *RP1* and *RP2* resistors too low (approx. below 1.5kΩ), the programmer is not able to provide the sufficient L level at *SDA/SCL* pins, you have to isolate *SDA* and *SCL* signals of programmed chip (by jumpers J1, J2, for example). At this case, the programmer provides *pull-up* resistors for *SDA/SCL* pins *(see Figure 3).*

A2, A1, A0 – Device address on IIC bus, hardwired to desired level *H/L*. control program provides an option to select this address which have to be sent during communication *(see Figure 5).*

WP (PRE, WC\) – Write Protect pin, must be set to inactive level while programming the device. The programmer uses this signal to test the WP pin level before programming the chip.

VCC – Power supply for programmed device must be supplied from target system. The programmer uses this signal only to test, if the target memory is powered. You can omit to connect this signal, and disable VCC sense.

GND – Common ground for programmer and target system.

Operating with device

Device operation options:

Most of the programmers offer an option to supply power for target system. If you want to use it, you must set up at least basic parameters. You can do it through menu *Device Options <Alt+O> - in next <Alt+O> (see Figure 4).*

Voltage level limitation of logical *H* signal is derived from target memory *VCC*, set in *Supply voltage* edit box *(value 3300mV, Figure 4)*.

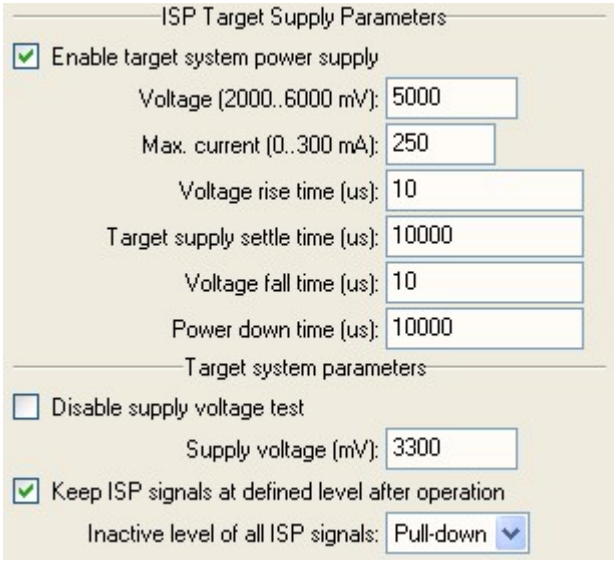

Figure 4. ISP target supply parameters setting <Alt+O>

If the programmed EEPROM have the *A2–A0* address inputs, you have to set the value in section *IIC special parameters <Alt+O>,* according to device address *A2, A1, A0* in system.

There exist a few devices which offer IIC address selection, and which haven't implemented this option in control program. In this case, programming algorithm has set combination *A2, A1, A0* to *[000]b.* Values quoted (in *DS*) as *X (Don't Care)* are also interpreted as *[0]b*.

In case of unfavourable communication conditions (longer wires, interfering environment, interference between signal from programmer and system...) you can decrease clock frequency used for communication by steps defined in IIC bus specification. Default value is set to maximum supported by selected EEPROM.

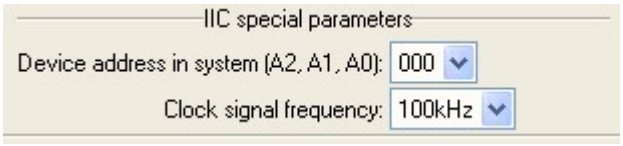

Figure 5. IIC special parameters setting <Alt+O>

For further description of ISP parameters, please take a look at menu *Help* by pressing the *<F1>* key, while the window *<Alt+O>* is opened.

Device info (Ctrl+F1):

The following window contains reduced information from this application note and details about pins assign for each programmer with short description of circuit design *(see Figure 6).*

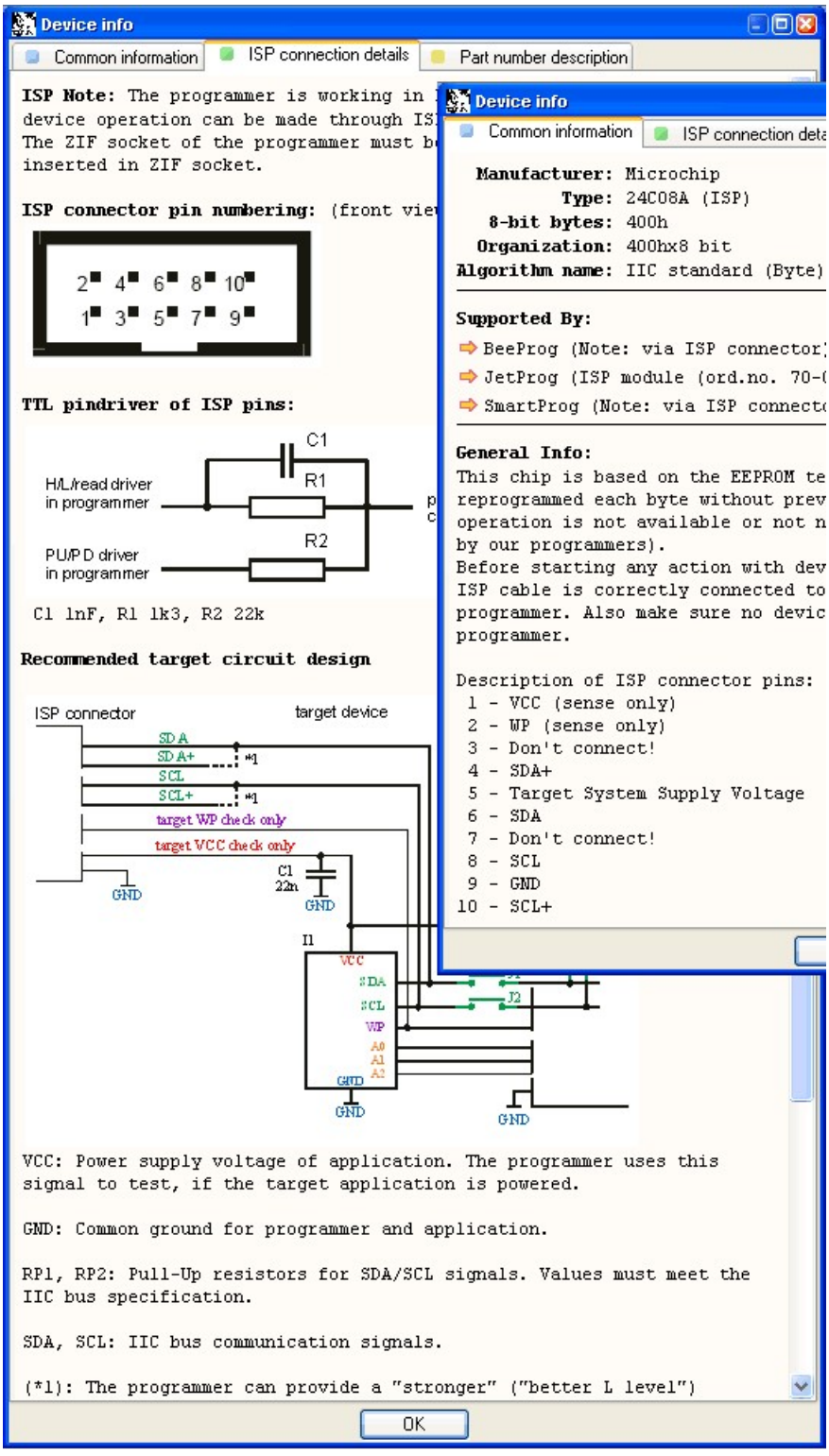

Figure 6. Device info

Good advices and troubleshooting

Connecting programmer to system:

Turn off power supply of system before connecting/ disconnecting programmer to/from system.

Before starting an operation:

Before starting an operation with target memory, please make sure, that the **ISP cable is correctly connected** to the target system and programmer. Also make sure that no device is inserted to *ZIF* socket of the programmer.

If you want to program the device, please make sure, that **signal *WP*** *(PRE, WC\)* **will not be active** during the action.

Details about pins assign for each programmer and short description of circuit design can be found in control program (*Device Info <Ctrl+F1>).*

Device pins marked *NC (Not Connected)* or *DC (Don't Connect!)* should be left unconnected. Also leave unconnected the pins of ISP connector marked ***"Don't Connect!".***

Correctly selected values of ***pull-up*** **resistors** on SDA/SCL wires of IIC bus can provide reliable signal level recognition (for both, programmer and system) and successfulness of desired operation. Please make sure, that your design meets IIC bus recommendations (see also *Adaptation of system for ISP,* page 4).

If something went wrong:

If programmer reports **signal interference error,** may be, a signal interference occurred between programmer and system. Please make sure, your design meets IIC bus recommendations. Check the minimal value of *PU* resistors on *SDA/SCL* wires from programmer's point of view (in order to programmer be able to put L level on the pin).

If you haven't yet **interconnected** the **signals** *SDA, SDA+ and SCL, SCL+* of ISP connector, please do that, and try to repeat desired operation.

If operation result still reports errors, please try to **decrease clock frequency** and repeat last operation *(<Alt+O>).*

Be aware, that longer ISP cable (longer than 20cm/0,7ft) may cause an unpredictable signal interference. Make sure you are using correct cable.

Used abbreviations

AN – *Application Note*.
DIP, SOIC, TSSOP, MLF, SON – type of device package.
EEPROM – *(Electrical Erasable Programmable Read Only Memory)* type of memory.
HW WP – *(Hardware Write Protect)* write protect feature. It's realized via appropriate signal level on device pin, not by setting some WP register.
IIC™ – *(Inter Integrated Circuit)* type of communication protocol, communication bus, IIC–bus™ is registrated trademark of *Philips Semiconductors Corporation.*
ISP – *(In System Programming)* programming of device inserted into system.
JTAG – *(Joint Test Action Group)* an acronym for Joint Test Action Group, is the usual name used for the IEEE 1149.1 standard for Test Access Port and Boundary Scan, primarily used for testing integrated circuits, but also useful as a mechanism for debugging embedded systems.
MW™ – *(MicroWire)* type of communication protocol, MICROWIRE™ is registrated trademark of *National Semiconductor, Corp.*
Open collector/drain – type of used interface, collector/drain of transistor creates an output. In order to be output able to set H level, the device needs to be supplied with constant PU on the pin.
Pull–Up (PU)/Pull–Down (PD) – *increase/decrease of signal level by connecting PU/PD* resistor to *VCC/GND*.
SPI™ – *(Serial Peripheral Interface)* type of communication protocol, SPI™ is registrated trademark of *Motorola Corporation.*
ZIF – *(Zero Insertion Force)* type of socket, used in programmer for better manipulation with device.

Revision history

05/2006:

Changes of figures:
- *Fig. 3 Circuit design – minor changes*
- *Fig. 6 Device info– minor changes*

06/2005:

Added sections:
- *"Revision history"* – this section.

Other:
- added abbreviation *"AN"*,
- changes in *"Device operation options"* section

02/2005:

Changes of terms:
- *"target device"* to AN specific *"serial EEPROM"* or *"EEPROM",*
- *"target application"* to *"target system".*

Changes of figures:
- *Fig. 3 Circuit design* – added comment marked as *"(*2)",*
- *Fig. 4 ISP target supply parameters setting – shows different values selected in edit box.*

01/2005:

Initial Release.