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AN–ELNEC–EN–ISP–HC11

Application note for In-System Programming of Motorola/Freescale HC11 MCUs

Introduction

The Motorola/Freescale HC11 family MCUs are high performance 8-bit microcontrollers with enhanced architecture and extended instruction set. Providing that intended *target system (application with embedded target MCU)* meets some circuit design requirements, these MCUs can be ISP programmed. **You should be familiar** with the device to know its operation and features before you start working with it.

In-system programming of HC11 MCU is performed while operating in special *"Bootstrap mode"*. This mode is entered after MCU reset, providing the *MODA, MODB* pins are at stable L level. *EXTAL* input is connected to external clock generator. External programming voltage is applied to Vpp/XIRQ\ input. Vpp value is set to 5V in case of programming and erasing any EEPROM memory area, 12V while programming an EPROM area. SCI pins *RxD, TxD* are used for serial communication. *VDD* and *VSS* are used to connection of supply voltage.

For detailed informations about all MCU configurable features, please refer to technical specification of programmed MCU – *Datasheet (DS).*

Signals:

Pin name	***Function***	***Description***	***Signal level***
VDD	power	supply voltage	5 (V)
VSS		ground	0 (V)
Vpp/XIRQ\	control	programming/interrupt voltage input	L, 5[1], 12[2] (V)
EXTAL		external clock input	H, L
MODA/LIR\		mode select input/debug output	L
MODB/Vstby		mode select/standby input	L
RESET\		MCU reset input	H, L
RxD	communication	SCI receiver, PD0	H, L, Pull-Up
TxD		SCI transmitter, PD1	

[1]- voltage of 5V is applied in case of programming any EEPROM memory area.
[2]- voltage of 12V is applied only in case of programming EPROM/OTPROM memory area.

Table 1. HC11 MCU ISP related signals description

Pinouts:

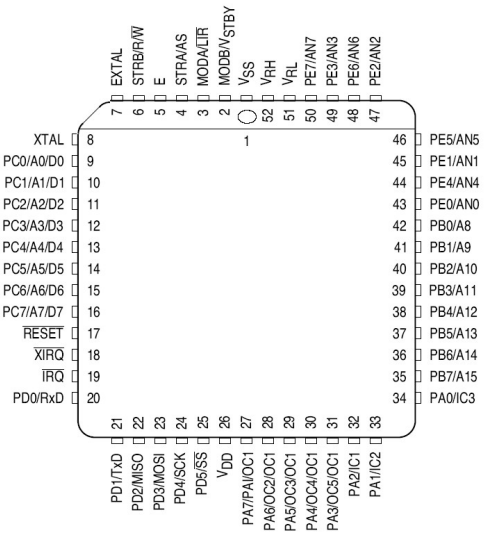

Figure 1. ***A series*** *PLCC52 package*

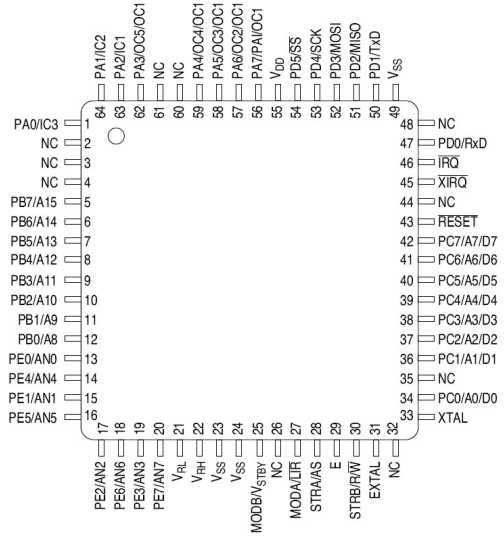

Figure 2. ***A series*** *QFP64 package*

Figure 3. ***A series*** *DIP48 package*

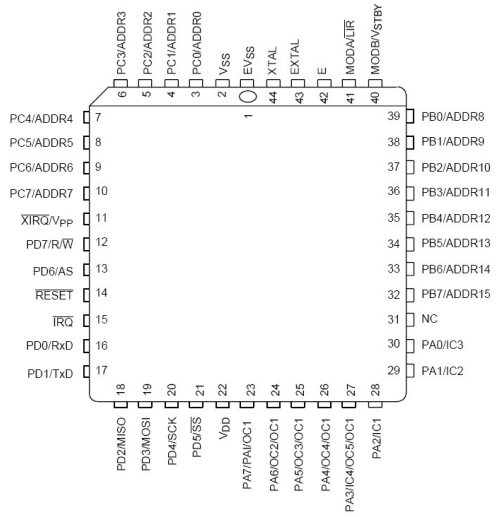

*Figure 4. **D series** PLCC44 package*

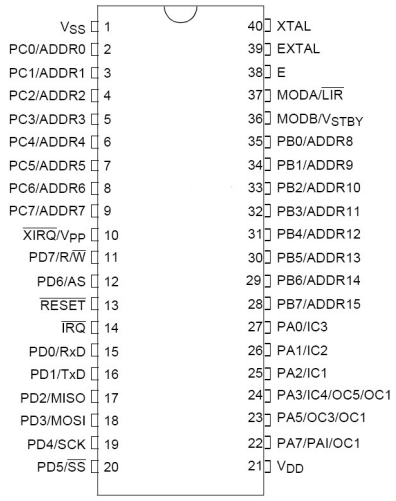

*Figure 5. **D series** DIP40 package*

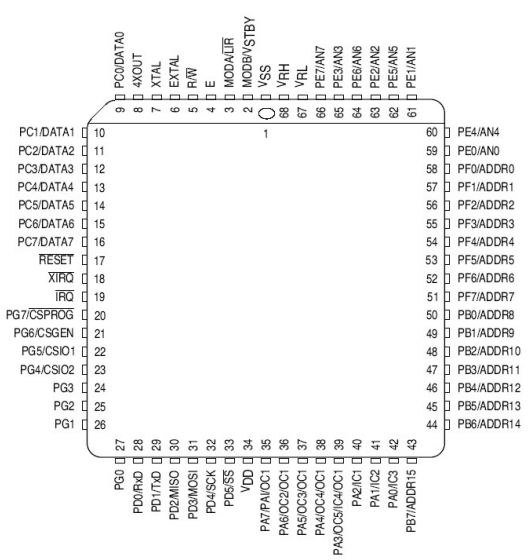

*Figure 6. **F series** PLCC68 package*

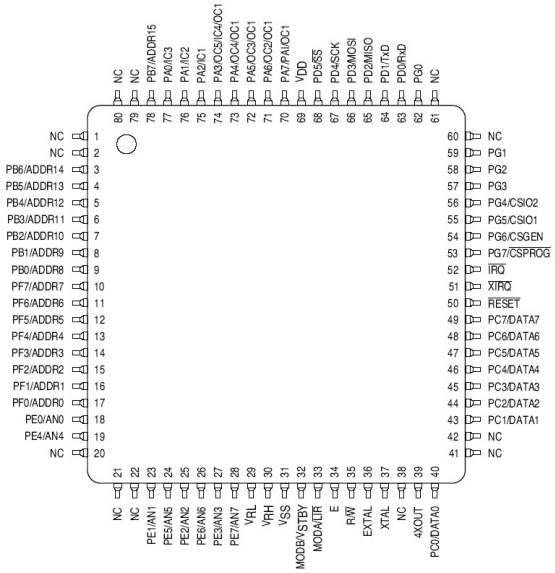

*Figure 7. **F series** QFP80 package*

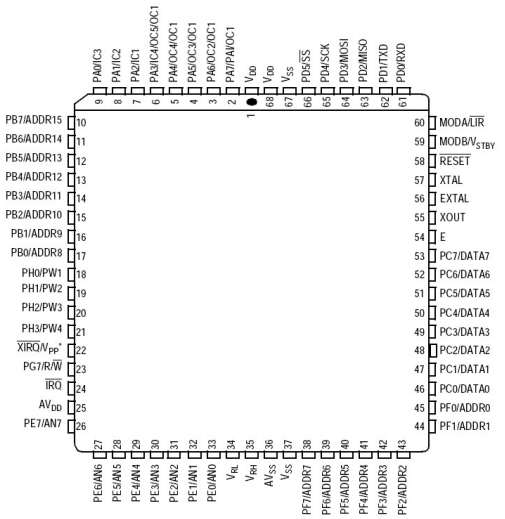

*Figure 8. **K series** PLCC68 package*

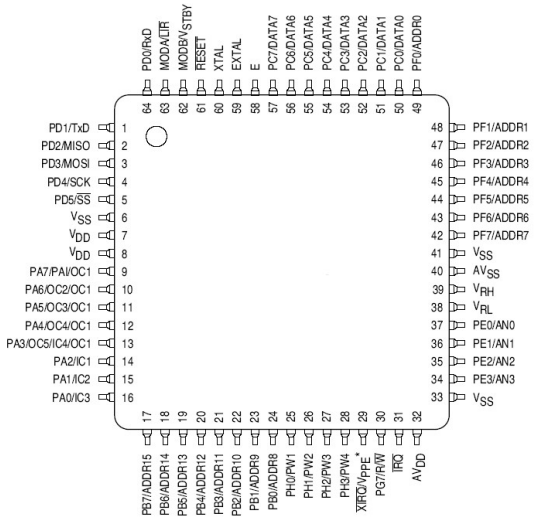

*Figure 9. **K series** QFP64 package*

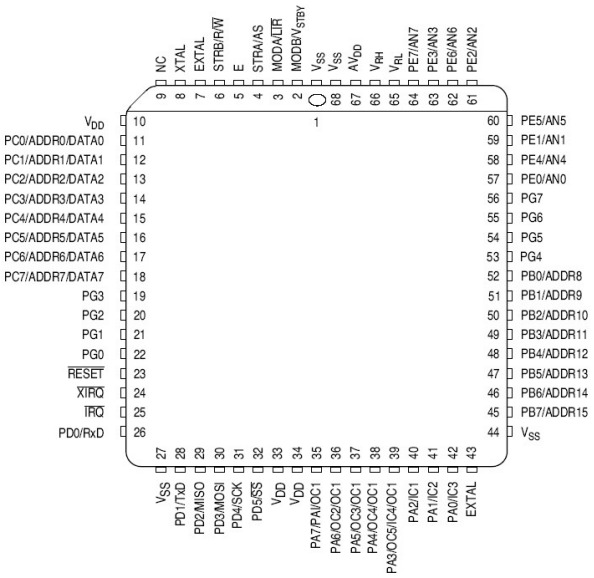

*Figure 10. **L series** PLCC68 package*

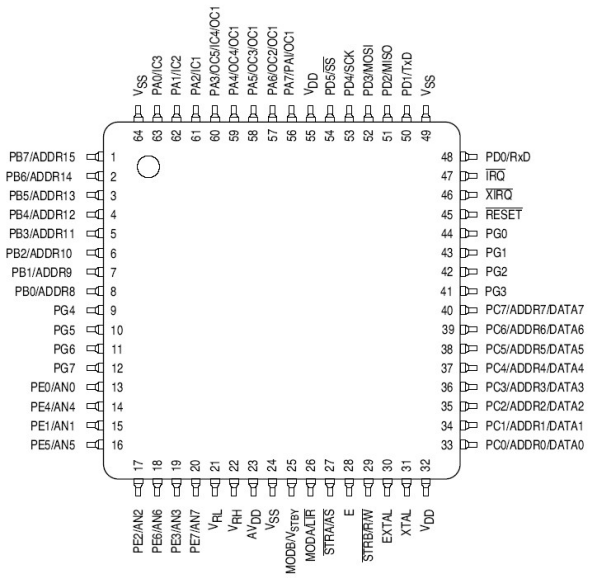

*Figure 11. **L series** QFP64 package*

Adaptation of target system for ISP

Following text contains **important notices** relating to correct ISP connection of in-system programmed MCU.

Respecting this, may prevent you from undesirable signal interference on pins *RxD, TxD, Vpp* of programmer and target system which often results in unsuccessful course of ISP operation.

Detailed information about ISP pin-driver capability and pins assign is listed in control program **PG4UW** of programmers *(Figure 6).*

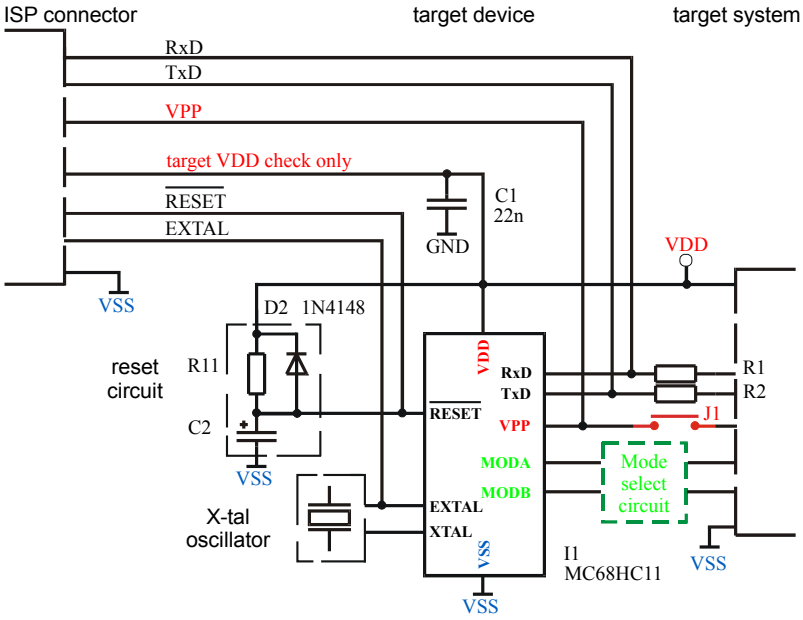

Figure 12. Circuit design

MODA/LIR\, MODB/VSTBY – Mode selection pins. They have to be in stable "L" level, during reset of MCU. It means, that voltage value mustn't exceed range <VSS-0.3V;0.2xVDD>. Mode select circuit should be adjusted accordingly to this condition. If the target system has even one of these pins directly connected to VDD, it's needed to disconnect it, and use weak Pull-Down resistor *(case 1, see Figure 13).* Other case, if these pins have a Pull-Up, your Pull-Down during ISP operation must be stronger, to meet previous declared condition, without disconnecting Pull-Up *(case 2, see Figure 14, Formula 1).*

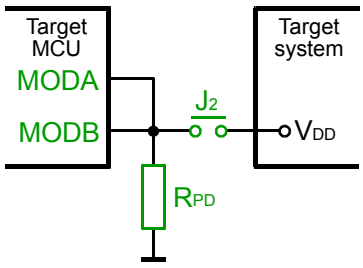

Figure 13. Mode selection, case 1

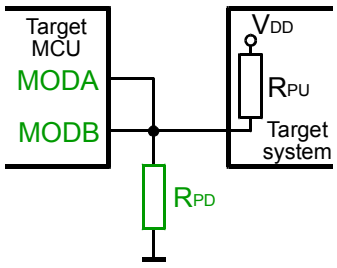

Figure 14. Mode selection, case 2

$$V_{RPD} \le 0.2 \cdot V_{DD}$$
$$\frac{V_{DD}}{R_{PU}+R_{PD}} \cdot R_{PD} \le 0.2 \cdot V_{DD} \quad \cdots \Rightarrow \quad \frac{R_{PD}}{R_{PU}+R_{PD}} \le 0.2$$
$$\boldsymbol{R_{PD} \le \frac{R_{PU}}{4}}$$

Formula 1-4. Understanding the relationship between R_{PD} and R_{PU}, case 2

VPP/XIRQ\– MCU programming voltage input signal. Also marked as XIRQ\. Be aware, that voltage of 12V is applied to this pin, but only during programming any EPROM area. Isolation circuit should be designed according to this. In case of programming EEPROM, serial isolating resistor could be sufficient. For EPROM programming, it is better to use jumper, rather than resistor.

Warning! Higher voltage during EPROM programming could harm your target system. All of these operations and target system adjustments are made on your own risk. We are not responsible of any damages in target system.

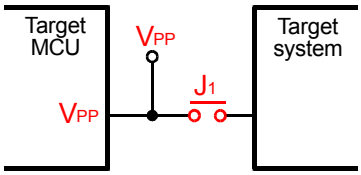

Figure 15. Connecting programmers Vpp, isolation circuit

EXTAL – MCU clock input signal. This pin can be over-driven by a programmer's oscillator, even if a crystal resonator circuit or RC network is connected to the EXTAL and XTAL pins.

RESET\ – during ISP operation, the Reset pin is considered as input only, extended reset circuit *(RC integrating circuit, R≥4,7kΩ, C≤1µF)* may be used.

RxD/PD0, TxD/PD1 – Communication pins, **TxD** of MCU is configured to standard CMOS output, **RxD** of MCU is configured as input, no Pull-Up resistor is needed during any ISP operation.

VCC – Power supply for programmed MCU must be derived from target system. The programmer uses this signal only to test, if the target MCU is powered. You can omit to connect this signal, and disable VCC sense.

GND – Common ground for programmer and target system.

Operating with device

Device operation options:

Most of the programmers offer an option to supply power for target system. If you want to use it, you must set up at least basic parameters. You can do it through menu *Device Options <Alt+O> - in next <Alt+O> (see Figure 4).*

Voltage level limitation of logical *H* signal is derived from target memory *VCC*, set in *Supply voltage* edit box *(value 3300mV, Figure 16)*.

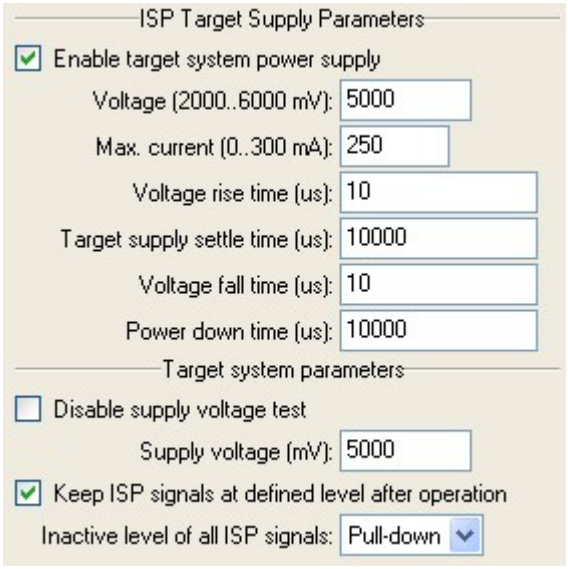

Figure 16. ISP target supply parameters setting <Alt+O>

For further description of ISP parameters, please take a look at menu *Help* by pressing the *<F1>* key, while the window *<Alt+O>* is opened.

Device info (Ctrl+F1):

The following window contains reduced information from this application note and details about pins assign for each programmer with short description of circuit design *(see Figure 6).*

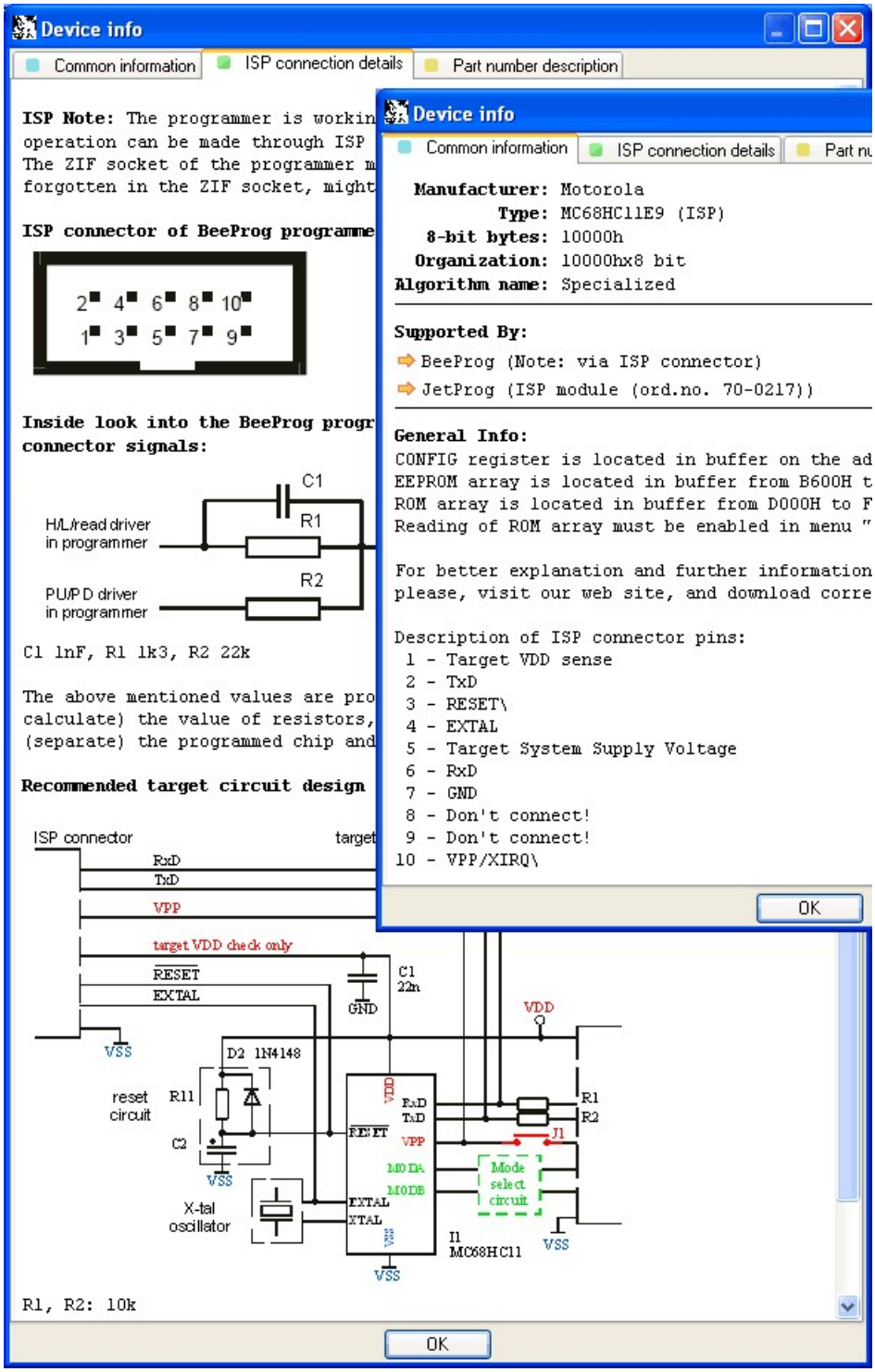

Figure 17. Device info

Connecting programmer to system:

Turn off power supply of system before connecting/ disconnecting programmer to/from system.

Before starting an operation:

Before starting an operation with target memory, please make sure, that the **ISP cable is correctly connected** to the target system and programmer. Also make sure that no device is inserted to *ZIF* socket of the programmer.

Details about pins assign for each programmer and short description of circuit design can be found in control program (*Device Info <Ctrl+F1>).*

Device pins marked *NC (Not Connected)* or *DC (Don't Connect!)* should be left unconnected. Also leave unconnected the pins of ISP connector marked ***"Don't Connect!".***

***Pull-down* resistors** on MODA, MODB pins of MCU must be correctly selected, for reliable entry to "Bootstrap Mode" and successfulness of desired operation. Please make sure, that your design meets our recommendations (see also *Adaptation of system for ISP,* page 6).

If something went wrong:

If programmer reports **signal interference error,** may be, a signal interference occurred between programmer and system. Please make sure, your design meets our recommendations and necessary isolation circuit were used on RxD, TxD pins. Check the maximal value of *PD* resistors on MODA, MODB (they must provide stable L level during MCU reset).

There may be a problem with MCU reset, if the RC integrating circuit connected to RESET\, have too big RC values. Please, try to decrease, or isolate it.

If operation result still reports errors, please try to **connect 22kΩ Pull-Up resistor** to pins IRQ and XTAL and repeat last operation.

Be aware, that longer ISP cable (longer than 20cm/0,7ft) may cause an unpredictable signal interference. Make sure you are using correct cable.

Used abbreviations

AN – *Application Note*.
CPU – *(Central Processing Unit).*
DIP, SDIP, QFP, TQFP, PLCC – type of device package.
EEPROM – *(Electrical Erasable Programmable Read Only Memory)* type of memory.
EPROM – *(Erasable Programmable Read Only Memory)* type of memory.
ISP – *(In System Programming)* programming of device inserted into system.
MCU – *(MicroController Unit) CPU with integrated peripherals and other features.*
Open collector/drain – type of used interface, collector/drain of transistor creates an output. In order to be output able to set H level, the device needs to be supplied with constant PU on the pin.
Pull–Up (PU)/Pull–Down (PD) – *increase/decrease of signal level by connecting PU/PD* resistor to *VCC/GND*.
Target MCU – *MCU to be programmed via ISP*.
Target system – *circuit, where the target MCU is embedded*.
ZIF – *(Zero Insertion Force)* type of socket, used in programmer for better manipulation with device.

Revision history

05/2006:

Changes of figures:

- *Fig. 12 Circuit design – minor changes*
- *Fig. 17 Device info– minor changes*

06/2005:

Initial Release.